REMARKS

The present application was filed on September 13, 2001 with claims 1-15. Claims 1, 13, 14 and 15 are the independent claims. In the outstanding Office Action, the Examiner: (i) rejected claims 1, 13 and 14 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,173,395 to Wisor et al. (hereinafter "Wisor"); (ii) rejected claims 2 and 3 under 35 U.S.C. §103(a) as being unpatentable over Wisor; and (iii) rejected claims 4-12 and 15 under 35 U.S.C. §103(a) as being unpatentable over Wisor in view of U.S. Patent No. 6,353,924 to Ayers et al (hereinafter "Ayers").

In this response, Applicants traverse the §102(e) and §103(a) rejections for at least the following reasons.

Regarding the §102(e) rejection of claims 1, 13 and 14, Applicant asserts that Wisor fails to teach or suggest all of the limitations in said claims for at least the reasons presented below.

It is well-established law that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Applicant asserts that the rejection based on Wisor does not meet this basic legal requirement, as will be explained below.

By way of example, the invention of amended independent claim 1 recites a method for tracing the execution path of a computer program comprising at least one module including a plurality of instructions, at least one of said instructions being a branch instruction, the method comprising the steps of identifying each branch instruction, evaluating each branch instruction to be one of true and false, and responsive to an evaluation of true, pushing a unique identifier into a predefined area of storage, wherein said unique identifier is associated with the instructions executed as a result of said evaluation of true. Claim 13 recites, *inter alia*, a pusher, responsive to an evaluation of true, for pushing a unique identifier into a predefined area of storage, wherein said unique identifier is associated with the instructions executed as a result of said evaluation of true. Claim 14 recites, *inter alia*, the step of instrumenting said instructions associated with an evaluation of true with a signature instruction, wherein said signature instruction causes a unique identifier to be pushed into a predefined area of storage upon execution of said true instructions at run-time.

Claim 15 recites, *inter alia*, a pusher for instrumenting said instructions associated with an evaluation of true with a signature instruction, wherein said signature instruction causes a unique identifier to be pushed into a predefined area of storage upon execution of said true instructions at run-time.

In accordance with an illustrative embodiment explained in the present specification, at paragraphs 48 and 49, upon execution of the program, as small, fixed size area called a signature area is defined. The signature area may contain up to a certain number of signature points. Each signature point comprises a unique 4 bit identifier. This identifier is, according to this illustrative embodiment, used to indicate the execution path or flow followed through the program. According to this illustrative embodiment, signature points are added to the signature area. For example, as explained at paragraph 57 of the present specification with respect to FIG. 5, case statement 1 is evaluated to TRUE such that 1 is pushed into the signature area 300. Execution then jumps to case statement 4, case statement 2, case statement 3, case statement 1, and finally to case statement 2. Accordingly, the corresponding identifiers are pushed into the signature area (1, 4, 2, 3, 1, 2). These numbers indicate which set of instructions have been executed at run-time and in what order. The signature information provides valuable insight into the behavior of the program. Should the program fail or behave erroneously, then the signature points can be used in subsequent problem diagnostics (paragraph 58).

The Office Action suggests that Wisor discloses all the features of the claimed invention. This is incorrect. Wisor does not disclose "pushing a unique identifier into a predefined area of storage, wherein said unique identifier is associated with the instructions executed as a result of said evaluation of true," as recited in claim 1; "a pusher, responsive to an evaluation of true, for pushing a unique identifier into a predefined area of storage, wherein said unique identifier is associated with the instructions executed as a result of said evaluation of true," as recited in claim 13; "instrumenting said instructions associated with an evaluation of true with a signature instruction, wherein said signature instruction causes a unique identifier to be pushed into a predefined area of storage upon execution of said true instructions at run-time," as recited in claim 14, or "a pusher for instrumenting said instructions associated with an evaluation of true with a signature instruction, wherein said

signature instruction causes a unique identifier to be pushed into a predefined area of storage upon execution of said true instructions at run-time," as recited in claim 15.

To the extent that the Office Action suggests that Wisor discloses such claimed features at column 3, lines 11-21, this is clearly incorrect. Column 3, lines 11-21, of Wisor state:

> When a test program is executed, a trace record is generated and stored in the BTHB [branch trace history buffer]. The trace record consists of full entries and bitmap entries. The full entries are generated for unconditional branches and other significant trace events. ("Full" entries, as used herein, are those entries which each correspond to a single branch or trace event.) The full entries contain information relating to the target addresses of the branches. The bitmap entries are generated for a series of conditional branches and contain individual bits which represent the taken or not-taken status of the branches.

Nothing in this passage from Wisor, nor any passage from Wisor, teaches or suggests "pushing a unique identifier into a predefined area of storage, wherein said unique identifier is associated with the instructions executed as a result of said evaluation of true," as recited in claim 1; "a pusher, responsive to an evaluation of true, for pushing a unique identifier into a predefined area of storage, wherein said unique identifier is associated with the instructions executed as a result of said evaluation of true," as recited in claim 13; "instrumenting said instructions associated with an evaluation of true with a signature instruction, wherein said signature instruction causes a unique identifier to be pushed into a predefined area of storage upon execution of said true instructions at run-time," as recited in claim 14, or "a pusher for instrumenting said instructions associated with an evaluation of true with a signature instruction, wherein said signature instruction causes a unique identifier to be pushed into a predefined area of storage upon execution of said true instructions at run-time," as recited in claim 15.

To the extent that the Office Action suggests that the bitmap entries of Wisor are equivalent to the unique identifier of the claimed invention, Applicant respectfully points out that such bitmap entries are expressly described as containing "individual bits which represent the taken or not-taken status of the branches." Thus, there is nothing unique about the bits since they merely represent whether a branch is taken or not taken.

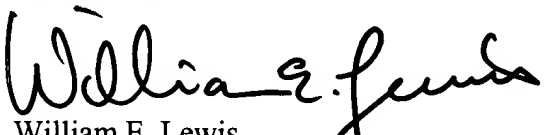
For at least these reasons, Applicant asserts that independent claims 1, 13 and 14 are patentable over Wisor.

Regarding the §103(a) rejection of claim 15, Applicants assert that Ayers fails to remedy the above-mentioned deficiencies of Wisor, and thus is patentable over the Wisor/Ayers combination for at least the above reasons. That is, Ayers also fails to disclose "pushing a unique identifier into a predefined area of storage, wherein said unique identifier is associated with the instructions executed as a result of said evaluation of true," as recited in claim 1; "a pusher, responsive to an evaluation of true, for pushing a unique identifier into a predefined area of storage, wherein said unique identifier is associated with the instructions executed as a result of said evaluation of true," as recited in claim 13; "instrumenting said instructions associated with an evaluation of true with a signature instruction, wherein said signature instruction causes a unique identifier to be pushed into a predefined area of storage upon execution of said true instructions at run-time," as recited in claim 14, or "a pusher for instrumenting said instructions associated with an evaluation of true with a signature instruction, wherein said signature instruction causes a unique identifier to be pushed into a predefined area of storage upon execution of said true instructions at run-time," as recited in claim 15. That is, among other deficiencies, there is no disclosure in Ayers of a unique identifier being pushed with respect to a true result in an evaluation of an instruction.

Regarding the §102(e) and §103(a) rejections of dependent claims 2-12, Applicants assert that such claims are patentable for at least the above reasons, and because such claims recite patentable subject matter in their own right.

In view of the above, Applicant believes that claims 1-15 are in condition for allowance, and respectfully requests withdrawal of the §102(e) and §103(a) rejections.

Respectfully submitted,



Date: August 19, 2004

William E. Lewis
Attorney for Applicant(s)
Reg. No. 39,274
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-2946